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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/941,180	08/27/2001	Hideyuki Harada	P/1071-1440	7067

7590 07/22/2005

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EXAMINER	
MAYES, MELVIN C	
ART UNIT	**PAPER NUMBER**
1734	

DATE MAILED: 07/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/941,180	HARADA ET AL.	
	Examiner	Art Unit	
	Melvin Curtis Mayes	1734	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 5-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 5-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

(1)

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

(2)

Claims 1, 5, 6, 10-12, 16, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gruenwald et al. 5,573,808 in view of Mikeska et al. 5,254,191.

Gruenwald et al. disclose a method of making a multilayer circuit having incorporated capacitance comprising: providing a structure comprising first and second electrode 1, 2 and either a printed dielectric layer or an already fired ceramic lamina 3 of high dielectric constant (capacitor having a sintered plate); arranging the structure between green ceramic sheets 11, 13, a green sheet having plated through holes and conductor tracks in contact with the electrodes; and firing the green sheets. Gruenwald et al. disclose that the dielectric can be applied in particularly thin layers with the result that large capacitances of the capacitor are possible. As shown in Figure 4, the fired ceramic lamina is of thickness less than the green ceramic sheets so as to be arranged between the green sheets (col. 1, line 31 – col. 2, line 51). Gruenwald et al. do not disclose providing at least one restriction layer on the green sheet laminate.

Mikeska et al. 5,254,191 teach that to reduce XY shrinkage during firing of a ceramic body, constraining layers of non-metallic inorganic solids which do not sinter during the sintering of the ceramic body are provided on at least one surface of the unfired ceramic body,

and after firing, the porous constraining layer(s) removed from the sintered ceramic body (col. 2, lines 38-64).

It would have been obvious to one of ordinary skill in the art to have modified the method of Gruenwald et al. for making a multilayer circuit having incorporated capacitance by providing removable constraining layers which do not sinter on the green sheet laminate, as taught by Mikeska et al, to reduce XY shrinkage during firing of the unfired ceramic body (green sheet laminate).

(2)

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gruenwald et al. 5,573,808 in view of Mikeska et al. 5,254,191 as applied to claim 5 above, and further in view of Branchevsky 6,252,761.

Branchevsky teaches that since there is a practical limit to the dielectric constant that can be achieved with single layer capacitors, it is desirable to have a multilayer capacitor embedded in a ceramic block to provide increased capacitance compares to single layer capacitors (col. 2, lines 36-51).

It would have been obvious to one of ordinary skill in the art to have modified the method of the references as combined by providing the capacitor structure as a multilayer capacitor, as taught by Branchevsky, to provide increased capacitance compared to a single layer capacitor. Providing the capacitor structure as a laminate of fired layers with internal conductor between layers would have been obvious to one of ordinary skill in the art to provide a multilayer capacitor instead of a single layer capacitor, as suggested by Branchevsky.

(3)

Claims 8, 9, 13-15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gruenwald et al. 5,573,808 in view of Mikeska et al. 5,254,191 as applied to claims 1 and 12 above, and further in view of JP 6-164150.

Gruenwald et al. disclose that the dielectric can be applied in particularly thin layers with the result that large capacitances of the capacitor are possible.

JP '150 teaches that in providing a ceramic multilayer substrate with a capacitor arranged between layers, the substrate can be made of green sheets which calcinate (sinter) at 900-1000°C and teach that the capacitor can provided to have a dielectric ceramic layer thickness of 12 micrometers (computer translation [0003], [0013]).

It would have been obvious to one of ordinary skill in the art to have modified the method of the references as combined by providing the fired dielectric ceramic capacitor lamina of thickness such as 12 micrometers, within the claimed range of 100 micrometer or less, as Gruenwald et al. disclose that the dielectric can be applied in particularly thin layers with the result that large capacitances of the capacitor are possible and JP '150 teaches that dielectric ceramic layer for a capacitor arranged in a ceramic multilayer substrate can be of thickness of 12 micrometers.

It would have been obvious to one of ordinary skill in the art to have further modified the method of the references as combined by providing the green sheets of composition that can be fired in the range of 900-1000°C, as JP '150 teaches that in providing a ceramic multilayer substrate with a capacitor arranged between layers, the substrate can be made of green sheets which calcinate (sinter) at 900-1000°C. Providing the green sheets which fire at 900-1000°C as

comprised of glass or ceramic and at least 5 weight percent glass, as claimed in Claims 14 and 15, would have been obvious to one of ordinary skill in the art, such as taught by Mikeska et al.

(4)

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gruenwald et al. 5,573,808 in view of Mikeska et al. 5,254,191 as applied to claim 1 above, and further in view of either Kodama et al. 5,277,723 or IBM Technical Disclosure Bulletin, February 1978 (entitled "Internal Capacitors and Resistors for Multilayer Ceramic Modules").

Kodama et al. teach that in producing a multilayer ceramic body having capacitors, a plurality of capacitors can be provided to be positioned inside the final laminate (Fig. 19).

IBM Technical Disclosure Bulletin, February 1978 teaches that resistors and capacitors can be built into a MLC substrate by inserting a ceramic disk between greensheets.

It would have been obvious to one of ordinary skill in the art to have modified the method of the references as combined by providing a plurality of capacitor structures or resistors and capacitors between the green ceramic sheets, as taught by Kodama et al. or IBM Technical Disclosure Bulletin, as known on the art to provide more than one capacitor or combination of capacitor and resistor in a multilayer ceramic body. Providing more than one capacitor or a combination of capacitor and resistor between the green sheets would have been obvious to one of ordinary skill in the art, as suggested by Kodama et al. or IBM Technical Disclosure Bulletin.

Response to Arguments

(5)

Applicant's arguments filed April 20, 2005 have been fully considered but they are not persuasive.

Applicant argues that the problem of warping or distortion during firing is addressed by providing a sintered plate having an area smaller than the area of the primary face of the green layer for the substrate on which the plate is arranged and disposing the sintered plate in the cavity formed in the green layer and providing the sintered plate thinner than the thickness of the green layer. Applicant argues that in Gruenwald, the capacitor forms a part of the surface of the green sheet and at not time is it between the abutting primary faces of sheet as called for in the claims.

(6)

Applicant claims in Claim 1 providing a laminate "wherein said sintered plate...is arranged between primary faces of a pair of adjacent green layers for the substrate which are in substantially parallel planes." This is the embodiment of Figures 1-4 where a capacitor is between adjacent green sheets, not the embodiment of Figure 6 where a green layer has a cavity as argued. In the embodiment of Claim 6, the capacitor is not arranged between "adjacent green layers" because there is a green layer having a cavity between the green layers. Claim 1 is limited to the embodiment of Figures 1-4.

With respect the Gruenwald, a laminate is formed having a fired capacitor between adjacent green sheets (layers). The laminate formed is essentially no different that that formed by

Applicant's embodiment of Figures 1-4 and the capacitor no more forms the surface a green sheet than Applicant's embedded capacitor forms a surface of a green layer in Figures 1-4.

With respect to Mikeska et al., the use of constraining layers to prevent XY shrinkage is known and would have been obvious to one of ordinary skill in the art to prevent XY shrinkage of the multilayer circuit of Gruenwald et al.

The prior art is replete with teachings or suggestions to provide fired or unfired single layer or multilayer capacitors in a multilayer ceramic substrate either between adjacent green sheets or within a cavity of a green sheet provided between green sheets, such as Gruenwald et al., IBM Technical Disclosure Bulletin, Kodama et al., Branchevsky, Steinle et al. 5,876,538, Ueda et al., JP 6-164150, JP 1-257318, JP 9-92977 or JP 8-213755, as well as teachings to use restriction layers to control XY shrinkage, such as Mikeska et al. and Kodama et al.

Conclusion

(7)

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

(8)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Melvin Curtis Mayes whose telephone number is 571-272-1234. The examiner can normally be reached on Mon-Fri 7:30 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris Fiorilla can be reached on 571-272-1187. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Melvin Curtis Mayes
Primary Examiner
Art Unit 1734

MCM
July 18, 2005